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FIELD-EFFECT TRANSISTOR

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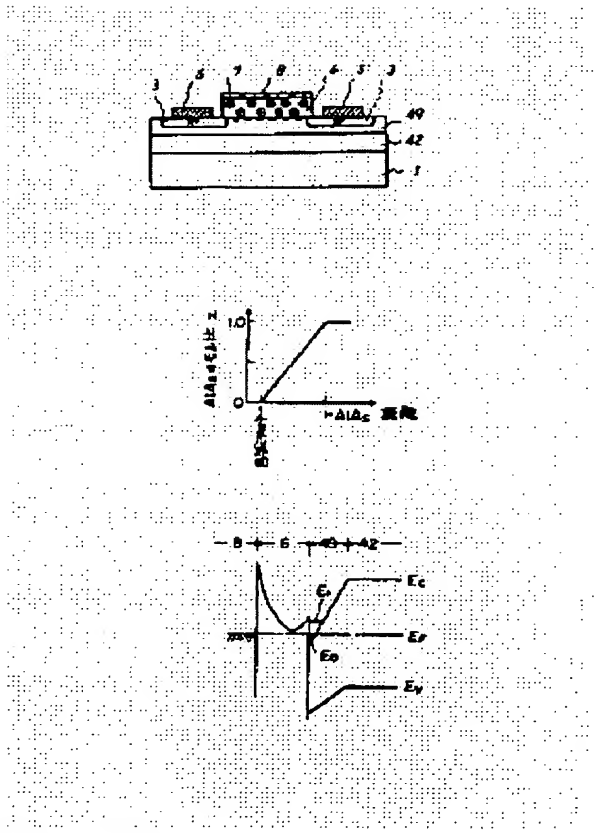
Abstract of **JP60223171**

PURPOSE:To obtain the field-effect transistor having excellent characteristics wherein the two-dimensionally accumulated condition of a high mobility electron is maintained by a method wherein a structure with which the electron affinity of a semiconductor crystal will be reduced from the surface where an electron layer will be formed toward the inner part of the semiconductor crystal in the direction reverse to a gate electrode. CONSTITUTION:Numeral 42 in the diagram is a non-doped high purity AlAs layer, numeral 49 is a non-doped high purity AlxGa1-xAs layer, and the molar ratio of AlAs is continuously changed from 0 to 1 from a channel interface to the AlAs layer 42. An example of distribution is shown by the diagram 5. The energy band in depthwide direction of a gate part in a thermally equilibrium state is as shown by the diagram 6. As a steep delta potential well is formed by a hetero interface and an AlxGa1-xAs layer 49, the energy difference between E0 and E1 is made larger, and accordingly, the probability of generation of an intersubband scattering between E0 and E1 of the electron supplied from the AlGaAs layer 6 whereon n type impurities are doped is small unit it is brought to a high energy state. Accordingly, a large mobility can be maintained in the same manner as the low voltage region even at a large source-drain voltage, thereby enabling to show excellent transportational characteristics.



Description of corresponding document: **US4740822**

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to semiconductor field effect devices having high speed and high frequency performances, and mc particularly to field effect transistors using one or more compound semiconductor materials.

2. Description of the Prior Art

Schottky gate field effect transistors (hereinafter, referred as MESFET's) for high frequency and high speed applications use GaAs having an electron mobility which is five to six times greater than Si. In such MESFET's, a GaAs layer is depc an insulator substrate and is heavily doped with N-type impurities, for example 10@17 cm@-3. A Schottky metal layer i contacted with the GaAs layer to form a gate electrode. The electron mobility, however, is limited to a low value, for exa 5,000 cm@2 /V.Sec at 300 DEG K., due to the scattering of ionized impurities.

To obtain an MESFET free from the effect of the scattering of ionized impurities, T. Mimura has proposed in U.S. Pat. N 4,424,525 a usage of heterojunction structure in which an AlGaAs layer doped with donor impurities is deposited on a h purity GaAs layer. A Schottky gate electrode is contacted with the AlGaAs layer. With the heterojunction structure, elec the impurity doped AlGaAs move into the high purity GaAs to form an electron accumulation layer, that is so-called twc dimensional electron gas, in the high purity GaAs at the interface between the high purity GaAs layer and the impurity d AlGaAs layer. The condition for forming the two-dimensional electron gas is that the electron affinity of the GaAs is hig the AlGaAs. By the relationship between the electron affinities, a potential well for forming the two-dimensional electro formed in the GaAs layer. Since the two-dimensional electron gas is produced in the high purity GaAs layer, the movem electrons is not interfered with by the ionized impurities and results in an improved high mobility such as 6,000 cm@2 / 300 DEG K. or 20,000 cm@3 /V.Sec at 77 DEG K. The mobility is superior at a low temperature.

The proposed heterojunction MESFET achieves the improvement of high frequency and high speed characteristics to a considerable extent. It, however, still has a problem at high field operation. If the electrons in the two-dimensional electr are excited so as to exceed the upper energy level of energy sub-bands by the high electric field between source and drai regions, the electron mobility lowers due to inter-sub-bands scattering. Especially, since the energy level difference betw energy sub-bands at the two-dimensional electron gas region in the proposed heterojunction MESFET is small, the inter- bands scattering is apt to occur even by a small electrical field between source and drain regions. Thus, the high frequen high speed operation of the proposed MESFET is easily deteriorated by the operating voltage between source and drain r

The proposed heterojunction MESFET has another problem. If the drain voltage VD is increased to exceed a voltage dif between the gate voltage VG and the gate threshold voltage VT, the potential well for forming the two-dimensional elec disappears near the drain region and the energy band structure of the channel region near the drain region declines from interface portion between the AlGaAs and GaAs layers to the inner portion of the GaAs layer. This allows the electron fl expand into the inner portion of the GaAs layer and results in an increment of drain-conductance in saturation operation. drain-conductance increment is remarkable in short-channel MESFET's.

SUMMARY OF THE INVENTION

The primary object of the present invention is to provide a field effect device having improved high frequency and high s performances.

Another object of the present invention is to provide a heterojunction field effect device having a stable high speed oper even at a high voltage operation.

A further object of the present invention is to provide a heterojunction field effect device having a small and stable drain conductance.

According to the present invention, there is provided a field effect device which comprises a gate electrode, a channel fo region in which a current channel is produced in accordance with a voltage applied to the gate electrode, and source and regions formed on both sides of the channel forming region, the channel forming region being made of a semiconductor having a graded electron affinity. The electron affinity is highest at the surface of said semiconductor material where the channel is formed and is decreased as the depth from the surface increases.

According to another aspect of the present invention, there is provided a heterojunction field effect device which compri channel region of a first semiconductor material having an electron affinity which is high at one surface thereof and grad lowers, an additional region of a second semiconductor material formed on the channel region in contact with the one su the first semiconductor material, the second semiconductor material having an electron affinity which is lower than the e affinity at the one surface of the first semiconductor material and being doped with impurities, a gate electrode formed o additional region to form a Schottky barrier with the second semiconductor material, and source and drain regions forme both sides of the channel region.

Since the electron affinity of the channel forming region of the first semiconductor material gradually lowers from the o surface to the inner portion, a deep potential well is produced at the interface of the first and second semiconductor mate The energy level difference between sub-bands of electron energy states becomes large in the deep potential well. There

inter-sub-bands scattering does not occur so long as the source-drain voltage difference does not become considerably la Thus, the high mobility is not deteriorated even in a high voltage operation.

Furthermore, since the channel forming region of the first semiconductor material has a lower electron affinity at the ins thereof than at its surface, the potential well for defining the region of current channel of the two-dimensional electron g not disappear near the drain region even if the drain voltage is considerably high. The path of electron flow is stably limi the potential well throughout the region between the source and drain regions. Thus, the drain-conductance increment dc occur in the saturation operation.

BRIEF DESCRIPTION OF THE DRAWING

The above and further objects, features and advantages of the present invention will become more apparent from the foll detailed description taken in conjunction with the accompanying drawings, wherein:

FIG. 1 is a sectional view of a heterojunction MESFET in the prior art;

FIG. 2 is an energy band diagram at the thermal equiblium at the section of the gate electrode portion of the heterojuncti MESFET in the prior art;

FIG. 3 is an energy band diagram at the section of the channel region near the drain region when a high voltage is applie drain region of the heterojunction MESFET in the prior art;

FIG. 4 is a sectional view of a heterojunction MESFET according to a first embodiment of the present invention;

FIG. 5 is a diagram showing a variation of mole ratio X in the Alx Ga1-x As which is used in the first embodiment of th present invention;

FIG. 6 is an energy band diagram at the section of the gate electrode portion of the heterojunction MESFET according tc first embodiment of the present invention;

FIG. 7 is a sectional view of a heterojunction MESFET according to the second embodiment of the present invention; an

FIG. 8 is an energy band diagram at the section of the gate electrode portion of the heterojunction MESFET according tc second embodiment of the present invention when a positive voltage is applied to the gate electrode.

A MESFET conventionally proposed is shown in the sectional view of FIG. 1. A semi-insulating GaAs substrate 1 is use starting material on which is deposited a high purity GaAs layer 2 doped with no impurity. N@+ -source and drain regio separately formed in the GaAs layer 2. On the surface of the GaAs layer 2 between the source and drain regions 3, Si-do AlGaAs layer 6 of N-type conductivity is deposited. Ionized Si-impurities 7 are distributed in the AlGaAs layer 6. A gat electrode 8 is formed on the AlGaAs layer 6 with a metal forming a Schottky barrier with the AlGaAs layer 6. Source an electrodes 5 are attached to the source and drain regions 3.

Here a normally-on type MESFET will be considered with FIGS. 1 and 2. The electron affinity of GaAs is larger than th AlGaAs. At the interface of the heterojunction between GaAs and AlGaAs layers 2 and 6, a triangular potential well is f inside the GaAs layer 2. Electrons in the Si-doped AlGaAs layer 6 are accumulated in the potential well to form a two-dimensional electron gas which contributes to the conductivity between the source and drain regions 3. The two-dimensi electron gas is modulated by the gate voltage.

In the potential well, quantum energy levels of electrons are formed. Here, for facilitating an understanding, the potentia of the potential well in the GaAs layer 2 is assumed to be constant. In other words, the electrical field in the potential we perpendicular direction is assumed to be a constant value Fs. The energy level Ei (i=0, 1, 2 . . .) measured from the lowe energy at the bottom of the conduction band of GaAs at the heterojunction interface can be approximately expressed as f ##EQU1## where m* is an effective mass of electron in GaAs, e is a charge of electron, and h is a value of Planck's con divided by 2.pi.. In FIG. 2, E0 and E1 are shown as examples.

In a usual operation where the electrical field is low such that the electron distribution function is not deviated from the t equiblium state, Fermi level EF exists between the energy levels E0 and E1 as shown in FIG. 2. Electrons move under a condition that their energies distribute between the energy level E0 and the Fermi level EF. If, however, the electrical fie becomes so large that the energies of electrons exceed the energy level E1, the so-called inter-sub-bands scattering occu lower the electron mobility. In the conventional structure of the heterojunction MESFET, the lowest level of the conduct band of GaAs sharply drops near the interface of the heterojunction but slowly increases at a portion far from the interfa causing a small electrical field in a direction perpendicular to the interface. This small electrical field makes the differen between the energy levels E0, and E1 and E2. Therefore, even by a relatively small electrical field between source and d regions, the lowering of electron mobility based on the inter-sub-bands scattering becomes notable and deteriorates the h

speed characteristics.

Another problem occurs when the voltage VD at the drain region becomes so high that it exceeds the difference between voltage VG at the gate electrode and the threshold voltage VT. In such a case, the energy band diagram at the channel re near the drain region changes as shown in FIG. 3 in which the potential well for forming the two-dimensional electron g disappears. Electrons which are shown in FIG. 3 by circles flow through a wide portion of GaAs layer 2, resulting in an of drain-conductance in saturation operation. This increment of the drain-conductance is remarkable in short channel FE is another cause for deterioration of high frequency and high speed characteristics.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Now, a first preferred embodiment of the present invention will be described with reference to FIGS. 4, 5 and 6. A semi-insulating GaAs substrate 1 is used as a starting material. A high purity AlAs layer 42 is deposited on the GaAs substrate molecular beam epitaxy with a thickness of 3,000 .ANG.. A high purity Alx Ga1-x As layer 49 is further deposited on th layer 42 by molecular beam epitaxy with a thickness of 3,500 .ANG.. The mole ratio X is continuously changed from 1 t That is, the Alx -Ga1-x As layer 49 is AlAs at the interface with the AlAs layer 49 and is GaAs at the top surface. Such of the mole ratio X is shown in FIG. 5 as one example. Source and drain regions 3 are separately formed in the Alx Ga1- layer 49 by highly diffusing N-type impurities. On a portion of the Alx Ga1-x As layer 49 between the source and drain 3, an N type AlGaAs layer 6 doped with donor impurities such as silicon with a concentration of 2.times.10@17 cm@-3 deposited by molecular beam epitaxy with a thickness of 900 .ANG.. In the N type AlGaAs layer 6, ionized donor impu are distributed. A metal such as aluminum which forms a Schottky barrier with the AlGaAs is deposited on the N type A layer 6 as a gate electrode. Source and drain electrodes 5 are formed in contact with the source and drain region 3, with a Au-Ge/Au which ohmically contacts the AlGaAs.

At the interface of the AlGaAs layer 6 and the Alx Ga1-x As layer 49, the Alx Ga1-x As layer 49 is GaAs. Here, the elec affinity of GaAs is larger than AlGaAs. Therefore, a triangular potential well is formed at the interface between the AlG layer 6 and the Alx Ga1-x As layer 49 but inside the Alx Ga1-x As 49. Electrons produced by the donor impurities in the AlGaAs layer 6 are accumulated in the potential well to form a two-dimensional electron gas. The two-dimentional elect is modulated by the voltage applied at the gate electrode 8. This operation is similar to the conventional MESFET show FIGS. 1, 2 and 3.

The energy band diagram at a portion of the gate electrode 8 and thereunder is shown in FIG. 6. The energy band structu Alx Ga1-x As layer 49 is different from the conventional MESFET. At the interface between the AlGaAs layer 6 and the Ga1-x As layer 49, the band structure is the same as the conventional MESFET, but the lowest energy of the conduction Alx Ga1-x As layer linearly rises up to the lowest energy of the conduction band of AlAs layer 42. As a result, a deep pc well is formed at the interface between the AlGaAs layer 6 and the Alx Ga1-x As layer 49 inside the Alx Ga1-x As layer Due to such a deep potential well, the difference between the energy levels E0 and E1 is wide, as is apparent from the ab explained equation (1). Therefore, electrons staying at the lower energy level E0 cannot move its energy state to the upp energy level E1, unless a considerably high electrical field is applied. In other words, unless a considerably high drain vc applied, the inter-sub-bands scattering does not occur and the original high electron mobility is maintained. The good hig and high frequency operation is kept at a high voltage operation.

Furthermore, as shown in FIG. 6, the lowest energy level of the conduction band of the Alx Ga1-x As rises up to a high level. For this reason, even if the drain voltage VD is so high that it exceeds the difference between the gate voltage VG threshold voltage VT, the potential well does not disappear near the drain region. This means, even by such high drain v VD, the path of current flow limited in the narrow potential well, results in no increment of drain-conductance in saturat operation. This effect becomes dominant in a shallow junction MESFET.

Other combinations of semiconductor materials applicable to the first embodiment are a combination of InP as the layer Ga1-x P as the layer 49 and AlGaAs doped with donor impurities as the layer 6 and a combination of GaAs as the layer Ga1-x As as the layer 49 and InAlAs doped with donor impurities as the layer 6. In each combination, the mole ratio X i small value at the interface with the layer 6 and increases in accordance with the distance from the interface with the lay that an electron affinity decreases in accordance with the distance from the interface with the layer 6.

The present invention may be applied to an insulated gate type heterojunction field effect device. FIGS. 7 and 8 are such examples. On a semi-insulating GaAs substrate 1, Gax In1-x As layer 72 is deposited by molecular beam epitaxy with a thickness of 2,000 .ANG.. The mole ratio X is "1" at the surface of the GaAs substrate 1 and is decreased linearly to "0.3 Source and drain regions 3 are separately formed by diffusing donor impurities with a high concentration. On the surface Gax In1-x As layer 72, SiO2 layer 76 is deposited with a thickness of 800 .ANG.. A metal of AuGe/Au alloy is selective deposited on the SiO2 layer 76 and the source and drain regions 3 as a gate electrode 8 and source and drain electrodes 5

The energy band diagram of the above-mentioned structure is shown in FIG. 8. The lowest energy level of the conductio of the Gax In1-x As layer 72 increases from the interface with the SiO2 layer 76 to the interface with the GaAs substrate application of positive voltage to the gate electrode 8, the lowest energy level of the conduction band of the Gax In1-x A 72 lowers below the Fermi level EF and produces a conductive channel of the two-dimensional electron gas.

According to such insulated gate field effect transistor, since the lowest energy band of conduction band of Gax In1-x A: up to a high value, the difference between energy levels E0 and E1 is wide, as is apparent from the equation (1). Therefo inter-sub-bands scattering does not occur even in high voltage operation and thus the original high electron mobility is maintained. Furthermore, due to the lowest energy level of conduction the band of the Gax In1-x As layer 72 which shar up to high value, the potential well for forming the two-dimensional electron gas does not disappear in the channel porti the drain region which is applied with a high voltage. The current channel does not spread near the drain region, resultin increment of drain-conductance in saturation operation even in a high voltage operation.

Suitable other semiconductor material may be changeable with the Gax In1-x As for the layer 72. Such suitable semicon material should have an electron affinity decreasing in accordance with the distance from the interface with the SiO2 lay An example is Inx Ga1-x P in which the mole ratio X increases in accordance with the distance from the interface with t layer 76.

Although some embodiments of the present invention have been explained hereinbefore, it is apparent that the present in is not limited to the above embodiments. Any suitable combination of semiconductor materials may be used, as explaine above. The present invention may be applicable to devices other than a transistor, for example a charge coupled device. charge coupled devices, the source and drain regions are charge injection and charge detection regions and a plurality of electrodes are aligned between the charge injection and charge detection regions.

Claims of corresponding document: **US4740822**

What is claimed is:

1. A field effect transistor comprising: a gate electrode applied with a gate voltage; an insulator film formed under said g electrode; a channel-forming semiconductor region formed under said gate electrode in contact with said insulator film, channel-forming semiconductor region primarily consisting of first and second semiconductor materials, said second semiconductor material having an electron affinity lower than said first semiconductor material, the content of said first semiconductor material in said channel-forming semiconductor region decreasing with distance from an upper surface th contacted with said insulator film, and said channel forming region forming a conductive channel in response to said gat voltage; and source and drain regions formed respectively on both sides of said channel-forming semiconductor region.

2. A field effect transistor as claimed in claim 1, wherein said first semiconductor material is selected from a group of In GaP, and said second semiconductor material is selected from a group of GaAs and InP.

3. A field effect transistor as claimed in claim 2, wherein the content of said second semiconductor material increases wi from zero at said upper surface, and the content of said first semiconductor material decreases with depth to thirty percer bottom of said channel-forming semiconductor region.

4. A field effect device comprising a channel forming region of a semiconductor material having an electron affinity whi lowers in accordance with the depth from one surface thereof, an insulator material formed on said one surface and a cor electrode formed on said insulator material, wherein said semiconductor material is selected from a group of Gax In1-x A Inx Ga1-x P in which the mole ratio x increases as the depth from said surface increases.

5. A field effect device comprising a channel forming region of a semiconductor material having an electron affinity whi lowers in accordance with the depth from one surface thereof, an insulator material formed on said one surface and a cor electrode formed on said insulator material, wherein said control electrode is a gate electrode and said field effect device comprises source and drain regions formed on both sides of said channel forming region, respectively, and wherein said semiconductor material is selected from a group of Gax In1-x As and Inx Ga1-x P in which the mole ratio x increases as depth from said one surface increases.

6. A field effect transistor comprising: a substrate of semi-insulating GaAs; a first semiconductor layer of pure AlAs fon said substrate; a second semiconductor layer of a semiconductor material formed on said first semiconductor layer, said semiconductor layer having a bottom surface contacting said first semiconductor layer and an upper surface, and said semiconductor material being Alx Ga1-x As in which the mole ratio X increases from 0 at said upper surface to 1 at said surface; source and drain regions separately formed in said second semiconductor layer to extend from said upper surfac third semiconductor layer formed on and contacting said upper surface of said second semiconductor layer located betw source and drain regions, said third semiconductor layer being formed of AlGaAs doped with donor impurities; and a ga electrode formed on and contacting said third semiconductor layer.

7. A field effect transistor comprising: a substrate of semi-insulating GaAs; a semiconductor layer formed on said substr semiconductor layer having an upper surface on the side opposite said substrate, and said semiconductor layer being fon Gax In1-x As in which the mole ratio x increases with depth from said upper surface from 0.3 to 1.0; source and drain re

separately formed in said semiconductor layer to extend from said upper surface; an insulator layer formed on said upper of said semiconductor layer located between said source and drain regions; and a gate electrode of metal formed on said insulator layer.

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⑤4発明の名称　電界効果トランジスタ

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発明の名称　電界効果トランジスタ

特許請求の範囲

半導体結晶表面に形成された電子層をチャネルとし、該チャネルを制御するゲート電極と、該チャネルにオーム接触するソース電極及びドレイン電極を具備した電界効果トランジスタにおいて、前記半導体結晶の電子親和力が、前記電子層が形成される表面から、前記ゲート電極と反対方向の前記半導体結晶の内部に向って減少する構造としたことを特徴とする電界効果トランジスタ。

発明の詳細な説明

（産業上の利用分野）

本発明は電界効果トランジスタ、特に表面電子チャネルを有する電界効果トランジスタ（FET）に関するものである。

（従来技術とその問題点）

近年、Siより電子移動度が5～6倍大きいGaAsを用いたショットキーゲート型FET（MESFET）が高周波・高速用素子として市販に供され、またこれを用いた集積回路の研究が盛んに行なわれている。しかしながら、上記MESFETでは多量のドナー不純物を含むn形半導体層をチャネルとしているため、イオン化不純物散乱によって電子の移動度および速度が制限されており、例えばGaAsでは電子濃度（ドナー不純物密度）10^{17} cm^{-3}で、300Kにおける電子移動度は5000 $cm^2/V.S$ 程度である。ところでノンドープの高純度GaAs上にドナー不純物をドープしたAlGaAs層を有するヘテロ接合構造ではAlGaAs中の電子が、より電子親和力の大きいノンドープGaAs側へ移動するためにヘテロ界面のGaAs中に電子蓄積層が形成されるが、これらの電子のほとんどは2次元電子ガスとして不純物のないGaAs中に存在するために、不純物散乱の影響が小さく、したがって特に低温において著しく移動

度が向上する。そこで、この電子蓄積層の電子濃度をAℓGaAs層上に形成されたショットキゲート電極で制御する構造のFETが注目されている。

第1図はそのFETの基本構造を示す断面図である。

1は半絶縁性GaAs基板、2はノンドープGaAs層、3はn^+コンタクト層、4は電子チャネル、5はソース電極、5'はドレイン電極、6はドナー不純物をドープしたAℓGaAs層、7はイオン化したドナー不純物、8はゲート電極である。ここで、このようなFETの例えばノーマリオン型素子を考えると、熱平衡状態でのゲート部の深さ方向のエネルギー帯図は第2図に示すようになる。ところで、この様な構造では第2図に示すようにヘテロ界面のGaAs側に電子が蓄積し、界面近傍では蓄積電子密度が大きいためにGaAs側のポテンシャルが大きく曲がり一種の三角ポテンシャルが形成される。この三角ポテンシャルに閉込められた電子はいわゆる2次元電子ガスとして存在し、界面に垂直方向の運動エネルギーが量子力学的効果で離散化され、いわゆる量子化エネルギー準位が形成される。今、簡単のため、三角ポテンシャルのGaAs側のポテンシャル勾配が一定、すなわち電界強度が一定値Fsをとるとすれば、ヘテロ界面GaAs伝導帯端から測ったこのエネルギー準位Ei（i=0, 1, 2……）は近似的に次式で表わされる。

$$Ei \simeq \left(\frac{\hbar^2}{2m^*}\right)^{\frac{1}{3}}\left[\frac{3}{2}\pi eF_s\cdot\left(i+\frac{3}{4}\right)\right]^{\frac{2}{3}} \quad \cdots\cdots (1)$$

ここで、m^*はGaAs中電子の有効質量、eは電子電荷、$\hbar$はプランク定数hを2πで割ったものである。第2図には一例としてE₀とE₁を示してある。さて、通常のFET動作でソース・ドレイン間の電界が小さく電子の分布関数が熱平衡状態からあまりずれないような場合には第2図に示すように、フエルミ準位E_FはE₀とE₁の間に存在し、電子はエネルギーがE₀とE_Fの間に分布した状態で運動する。しかしある程度電界が大きくなり電子のエネルギーがE₁を越えるようになると、E₀の準位とE₁の準位間で、いわゆるサブバンド間散乱が起り電子の移動度が低下するという問題が生じる。従来構造のFETでは第2図に示したように電子が蓄積している界面近傍ではポテンシャルの曲りが大きいが、界面より離れたGaAs中では蓄積電子密度に対して空間電荷密度が小さいためにバンドの曲りが小さく、従って界面に垂直方向の電界も小さいことより式(1)から判るようにE₀とE₁、あるいはE₁とE₂等のエネルギー差が小さい。このために比較的小さなソース・ドレイン間電界でもサブバンド間散乱による電子移動度低下が顕著となり素子の高速動作という観点からは大きな問題となっている。

上記FET構造の別の問題点は、ドレイン電圧をV_D、ゲート電圧をV_G、ゲート閾値電圧をV_Tとするとき、ドレイン電圧を増加させて$V_D > V_G - V_T$となった状態では、チャネルのドレイン端に近い場所の界面のエネルギー帯図は第3図のようになり、電子に対するポテンシャルエネルギーがGaAs中で界面より内部に向って、低くなった状況となることである。

すなわち、電子（白丸）は界面から離れてGaAs層内部を走行するようになり、実効的な電流路がドレイン側で拡がる為に、特に短チャネルFETにおいて飽和特性のドレインコンダクタンスの増大をきたし、FET特性を劣化させる。

以上はヘテロ接合を有するFETについて説明したが、同様なことは絶縁ゲート形FET（MISFET）など表面チャネルを有するFETに共通の問題である。

（発明の目的）

本発明の目的は、上述のような問題点を解消し、高移動度電子の2次元的蓄積状態を維持した良好な特性を有する電界効果トランジスタを提供することにある。

（発明の構成）

本発明によれば、半導体結晶表面に形成された

電子層をチャネルとし、該チャネルを制御するゲート電極と、該チャネルにオーム接触するソース電極及びドレイン電極を具備した電界効果トランジスタにおいて、前記半導体結晶の電子親和力が前記電子層が形成される表面から、前記ゲート電極と反対方向の前記半導体結晶の内部に向って減少する構造としたことを特徴とする電界効果トランジスタが得られる。

（実施例）

以下本発明を実施例により詳細に説明する。

第4図は本発明の一実施例を示す電子チャネルの電界効果トランジスタの構造の断面図で、第1図と同一番号のところは同一内容を表わし、42はノンドープ高純度のAℓAs層、49はノンドープ高純度$Aℓ_xGa_{1-x}As$層でAℓAsのモル比xをチャネル界面から42のAℓAs層に向って0から1まで連続的に変化させたもので、分布の一例を第5図に示す。熱平衡状態におけるゲート部の深さ方向のエネルギー帯図は第6図に示すようになる。

ヘテロ界面と$Aℓ_xGa_{1-x}As$層49により急峻な三角ポテンシャル井戸が形成されるために、前述の議論から明らかな様に、この場合はE₀とE₁のエネルギー差が大きく、従ってn型不純物をドープしたAℓGaAs層6から供給された電子はかなり高エネルギーの状態になるまでE₀とE₁の間でサブバンド間散乱を起す確率が小さい。この為に、大きなソース・ドレイン間電圧でも低電圧領域と同様に大きな移動度を保持し良好な輸送特性を示すこととなる。

さらに本構造では、たとえドレインバイアスの大きい動作状態においても、ソースからドレインにわたってチャネル電子の基板側には$Aℓ_xGa_{1-x}As$層49からなるポテンシャル障壁が厳に存在するために、電子はヘテロ界面近傍を走行する。したがって従来例のような電流拡がり効果によるドレインコンダクタンスの増大劣化がない。またソース側のn^+コンタクト層から注入される電子は、ほとんどが電子親和力の大きいヘテロ界面よりに注入されるために、ヘテロ界面より基板側のノンドープ高純度$Aℓ_xGa_{1-x}As$中を流れる電子による空間電荷制限電流の影響はきわめて小さく、したがって従来例の短チャネル素子で顕著であった基板側を流れる電流によるドレインコンダクタンスの増加も防止できる。

以上説明した本発明による電界効果トランジスタの第一の実施例は以下のように製作される。

例えば、半絶縁性GaAs基板上に分子線エピタキシー法によりノンドープ高純度AℓAs層を3000Å、ノンドープ高純度$Aℓ_xGa_{1-x}As$層を第5図に示したAℓAsのモル比xの分布に従って3500Å、さらに有効ドナー不純物密度$2\times10^{17}\ cm^{-3}$のAℓGaAs層を900Å成長する。次いでイオン注入法によりソースおよびドレインにn^+領域を形成し、ゲート電極およびソース、ドレイン電極を通常の方法により形成すれば素子が完成する。

以上はヘテロ接合を有するFETについて説明したが本発明は絶縁ゲートを有するFET (MISFET)についてもきわめて良好な特性を有する素子を実現させる。第7図はMISFETに適用した場合の構造図で、例えば半絶縁性GaAs基板1上に$Ga_xIn_{1-x}As$を分子線エピタキシー法によりxを1から0.3まで変化させて2000Å成長し、その上に例えばCVD SiO_2膜76を800Å成長しさらに窓開けを施してイオン注入法によりn^+コンタクト層3を形成して通常の方法でゲート電極及びソース・ドレイン電極を形成して素子が完成する。ゲートに正バイアスを印加してチャネルに電子を誘起した時のエネルギー帯図を第8図に示す。

本構造では実施例1で説明したと同様な特徴および効果を有するとともに、さらに例えばチャネルが形成される$Ga_xIn_{1-x}As$層のGaAsのモル比xが自由に選択できる特徴を有する。ここではGaAsを基板とした場合の$Ga_xIn_{1-x}As$層を一例として示したが、他の基板及び混晶半導体層に本発明が適用できることは明らかであろう。

（発明の効果）

以下の説明において詳述した様に、本発明によ

れば従来技術における電子チャネルの拡がりによる問題点のない極めて良好な動作特性を有する電界効果トランジスタが実現され、特に短チャネルにおいて高性能な電界効果トランジスタが実現できる。さらに前記本発明は個別素子のみならず、集積回路およびオプトエレクトロニクス関係へも応用することができる。

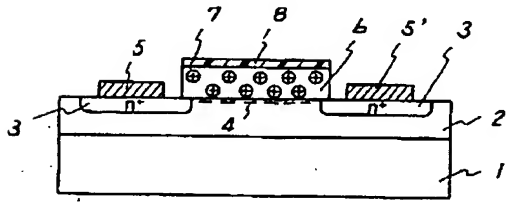
図面の簡単な説明

第1図、第2図、第3図はヘテロ接合を利用したFETの従来例を示すもので第1図は構造、第2図はゲート部の深さ方向での熱平衡状態におけるエネルギー帯図、第3図はドレインに高電圧を印加した場合のゲートのドレイン端での深さ方向のエネルギー帯図である。また第4図、第5図、第6図、第7図、第8図は本発明によるFETの一実施例を説明するための図で、第4図はヘテロ接合を利用したFETの構造、第5図は$A\ell_xGa_{1-x}As$層中$A\ell As$のモル比分布、第6図は熱平衡状態でのエネルギー帯図、第7図はMISFETの構造、第8図はゲートに正電圧を印加した時のエネルギー帯図を示す。

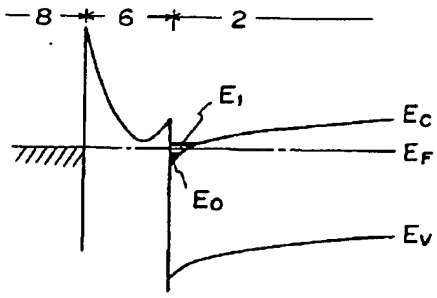
図において、

1……半絶縁性GaAs基板
2……ノンドープ高純度GaAs層
3……n^+コンタクト層
4……電子蓄積層
5……ソース電極
5'……ドレイン電極
6……ドナー形不純物ドープ$A\ell GaAs$層
7……イオン化ドナー
8……ゲート電極
42……ノンドープ高純度$A\ell As$層
49……ノンドープ高純度$A\ell_xGa_{1-x}As$層
72……ノンドープ高純度$Ga_xIn_{1-x}As$層
76……ゲート絶縁膜
E_F……フェルミレベル
E_C……伝導帯
E_V……価電子帯
白丸……電子

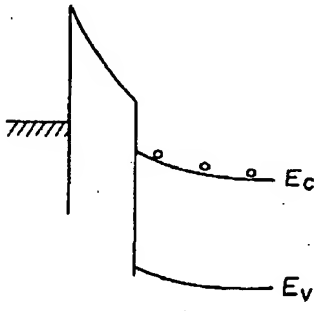
第1図



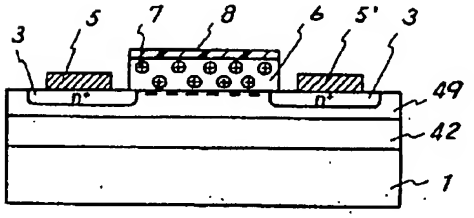
第2図



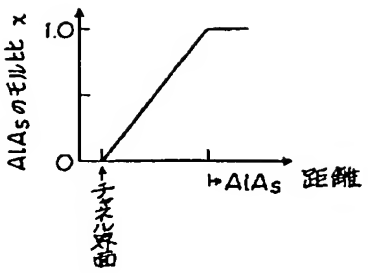
第3図



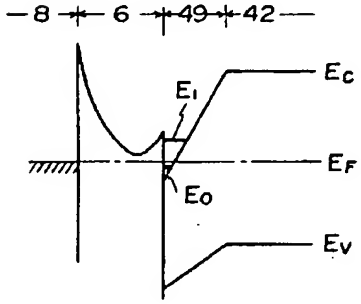
第4図



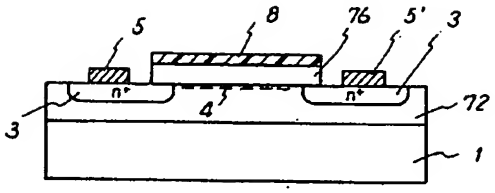
第 5 図



第 6 図



第 7 図



第 8 図